Design of a Reference Voltage Source Based on Complementary Threshold Voltage of NMOS and PMOS

Shulin Liu[*1], Jing Ji[2]

[*1, 2] School of Electrical and Control Engineering, Xi'an University of Science & Technology
Xi'an, China

[*1]lsigma@163.com; [2]jj2007032 @126.com

Abstract

A new reference voltage source is presented according to the linear relationship between temperature and the threshold voltages of NMOS and PMOS. Compared with ordinary CMOS band-gap reference, the designed circuit doesn't need parasitic transistor, and the process parameters are easier to control. In addition, the output reference voltage has a theoretical zero temperature coefficient at any point within circuit normal operating temperature range, and its value can be arbitrarily adjusted. The simulation results indicate that the circuit has better temperature stability and high power supply rejection ratio.

Keywords

Reference Voltage Source; NMOS; PMOS; Threshold Voltage

Introduction

As an important unit module in analog circuits, reference voltage source is widely used in oscillator, error amplifier, DAC and ADC, etc. Its output voltage quality directly affects the stable and reliable work of relevant circuit. The output voltage of ideal reference voltage source should be reliable and has excellent anti-interference ability. Meanwhile, it doesn't change with temperature and power fluctuations, and has nothing to do with the process parameters.

At present, band-gap reference is usually used to generate reference voltage, which gets a voltage with zero temperature coefficient through the weighted sum of positive temperature coefficient of thermal voltage V_T and negative temperature coefficient of transistor base - emitter junction voltage V_{BE} in some way. However, since the nonlinearity of V_{BE} temperature coefficient, reference voltage has a zero temperature coefficient only at a point within circuit normal operating temperature range. In order to obtain more accurate reference voltage, it is necessary to provide second-order or even higher-order compensation, but this increases the difficulty in circuit design and can not fundamentally solve the problem of nonlinear temperature coefficient of V_{BE}. In addition, V_{BE} is mostly generated by parasitic transistor in CMOS process, which leads to larger area, higher power consumption and also affects the whole circuit performance.

To this end, a full CMOS reference voltage source without parasitic transistor is presented. It utilizes the complementation of the linear relationship between MOS threshold voltages and temperature to generate a temperature-independent reference voltage. Not only can it have a zero temperature coefficient at any point within circuit normal operating temperature range, but also the voltage value can be arbitrarily adjusted.

The Principle of Reference Voltage Based on Complementary Threshold

Firstly, the temperature characteristics of MOS related parameters are analyzed. MOSFET can be biased in the linear region or the saturation region during normal operation. The channel length modulation effect can be ignored if channel is long. At this point, in the linear region, the current is:

$$I_{DS} = \frac{\mu \cdot C_{ox}}{2}\left(\frac{W}{L}\right)\left[2 \cdot \left(\left|V_{GS}\right| - \left|V_{th}\right|\right) \cdot \left|V_{DS}\right| - V_{DS}^2\right] \quad (1)$$

The current in the saturation region is:

$$I_{DS} = \frac{\mu \cdot C_{ox}}{2}\left(\frac{W}{L}\right)\left(\left|V_{GS}\right| - \left|V_{th}\right|\right)^2 \quad (2)$$

In (2), μ is carrier mobility, C_{ox} is the gate capacitance per unit area, (W/L) is the ratio of channel width to length, V_{th} is threshold voltage. Among these parameters, only V_{th} and μ are related to temperature.

According to the model BSIM3v3, the relationship between threshold voltage V_{th} and temperature is:

$$V_{th}(T) = V_{th(Tnorm)} + \left(K_{T1} + \frac{K_{t1l}}{L_{eff}} + K_{T2}V_{bseff}\right) \cdot \left(\frac{T}{T_{norm}} - 1\right) \quad (3)$$

T_{norm} is the temperature at which MOS parameters are extracted, $V_{th(Tnorm)}$ is the threshold voltage of MOSFET under the temperature T_{norm}, K_{T1} is temperature coefficient for threshold voltage, K_{t1l} is channel length dependence of the temperature coefficient for threshold voltage, L_{eff} is effective channel length,K_{T2} is body-bias coefficient of V_{th} temperature effect , V_{bseff} is effective substrate bias voltage. As can be seen from （3）, V_{th} is linear with temperature. On the contrary, μ has a nonlinear relationship with temperature, the nonlinear functional relationship is given by:

$$\mu(T) = \mu_{0(Tnorm)}\left(\frac{T}{T_{norm}}\right)^{\mu te} \quad (4)$$

Where, $\mu_{0(Tnorm)}$ is the carrier mobility under temperature T_{norm} , μ_{te} is temperature index for carrier mobility, generally in the range of -1.5 to -2.0. If the reference voltage is related to μ, the situation is similar to V_{BE}. A zero temperature coefficient is difficult to be obtained within the entire temperature range because μ is nonlinear with temperature. Therefore, some kind of circuit is conceived to offset the influence of μ and generates two voltages which have a linear relationship with threshold voltages of NMOS and PMOS respectively, and then the temperature-independent reference voltage is obtained by using weighted summation. Principle is shown in FIG.1:

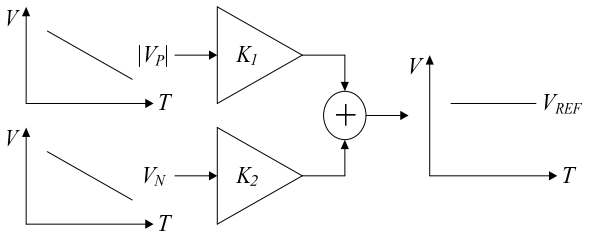

FIG.1 THE SCHEMATIC OF REFERENCE VOLTAGE BASED ON COMPLEMENTARY THRESHOLD

Where, $|V_P|$ and V_N have linear relationship with threshold voltages of PMOS and NMOS respectively, which are also linear with temperature. As long as the weighting coefficient is set reasonable, not only can the reference voltage V_{REF} be independent of temperature, but also the value can be set as required, the value is:

$$V_{REF} = K_1V_P + K_2V_N \quad (5)$$

Specific Circuit Design

A specific circuit is designed to counteract mobility μ and produce voltages of V_P and V_N, shown in FIG.2, where, Module 1 is voltage V_P generating circuit, Module 2 is voltage V_N generating circuit, Module 3 is the weighted summation circuit. The temperature coefficients offset each other after V_P and V_N making the weighted summation. Finally, a reference voltage with zero temperature coefficient is obtained.

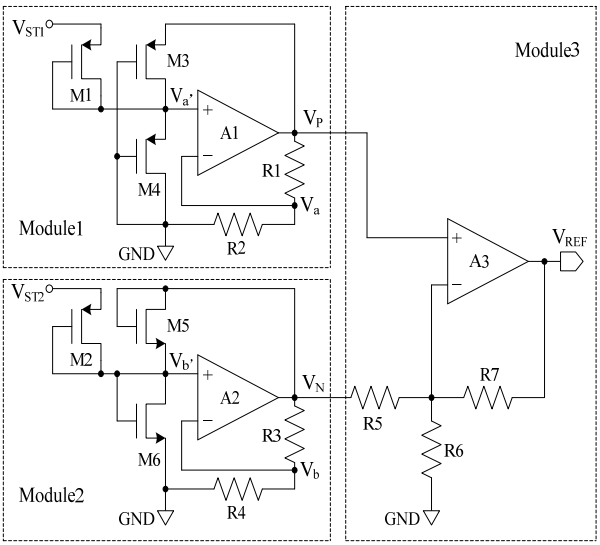

FIG.2 THE CIRCUIT MODULE OF REFERENCE VOLTAGE SOURCE BASED ON COMPLEMENTARY THRESHOLD

Design of Voltage V_P Generating Circuit

All node voltages in Module 1 are zero before power-on. After power-on, the non-inverting /inverting input and output voltages of amplifier A1 are still zero, M3 and M4 are closed and remain that state without additional excitations. Therefore, It is necessary to enhance the voltage V_a' by adding start - up transistor M1 to make the circuit work normally. When V_a' is stable, its voltage must be higher than PMOS threshold $|V_{thp}|$ in order to make M4 turned on, but that results in M3 working in linear region. If voltage V_{ST1} is set to a value greater than $|V_{thp}|$ and less than $|2V_{thp}|$, M1 is turned off after the circuit is stable. Operational amplifier A1 contains a negative feedback made of R1, R2 and a positive feedback made of M3, M4.Through reasonably setting R1, R2 value and M3, M4 width to length ratio to make negative feedback effect is much larger than positive feedback, so that A1 is in the deep negative feedback state. If temporary excluding the input offset voltage, we get Equation (6):

$$V_{a'} \approx V_a = \frac{R_2}{R_1 + R_2}V_P \quad (6)$$

M4 is always in the saturation region because it is connected as a diode. Since the currents through M5 and M6 are equal, and according to (1) and (2), the following equations can be obtained:

$$\begin{cases} I_3 = \dfrac{\mu_p C_{ox}}{2}\left(\dfrac{W}{L}\right)_3\left[2\cdot(V_P + V_{thp})(V_P - V_{a'}) - (V_P - V_{a'})^2\right] \\ I_4 = \dfrac{\mu_p C_{ox}}{2}\left(\dfrac{W}{L}\right)_4 (V_{a'} + V_{thp})^2 \\ I_3 = I_4 \end{cases} \tag{7}$$

Define $\alpha_1 = \dfrac{R_2}{R_1 + R_2}$, $\beta_1 = \left(\dfrac{W}{L}\right)_4 \Big/ \left(\dfrac{W}{L}\right)_3$, taking (6) into(7) can obtain:

$$V_P = \frac{1 - \alpha_1(1 + \beta_1) + (1 - \alpha_1)\sqrt{1 + \beta_1}}{1 - \alpha_1^2(1 + \beta_1)} V_{thp} \tag{8}$$

As can be seen, carrier mobility μ is offset. Although R1 and R2 are related to temperature, but through the reasonable layout design to make they are consistent with the changes of process and temperature, α_1 and β_1 can be considered to be constants independent of temperature. Because V_{thp} is linear with temperature, so voltage V_P is a linear function about temperature and can be adjusted by setting different α_1 and β_1.

Design of Voltage V_N Generating Circuit

Similarly, in Module 2, M2 is the start - up transistor. When circuit is stable, M5 and M6 that connected into diode forms are both working in saturation region, voltage V_b' is higher than NMOS threshold V_{thn}. If voltage V_{ST2} is set to a value greater than $|V_{thp}|$ and less than $V_{thn} + |V_{thp}|$, M2 is turned off after circuit is stable. Through reasonably setting R3, R4 value and M5, M6 width to length ratio, operational amplifier A2 can work in the deep negative feedback state. If temporary excluding the input offset voltage, we get Equation (9) too:

$$V_{b'} \approx V_b = \frac{R_4}{R_3 + R_4} V_N \tag{9}$$

Because the currents through M5 and M6 are equal, and according to Equation (2), we can obtain:

$$\begin{cases} I_5 = \dfrac{\mu_n C_{ox}}{2}\left(\dfrac{W}{L}\right)_5 (V_N - V_{b'} - V_{thn})^2 \\ I_6 = \dfrac{\mu_n C_{ox}}{2}\left(\dfrac{W}{L}\right)_6 (V_{b'} - V_{thn})^2 \\ I_5 = I_6 \end{cases} \tag{10}$$

Define $\alpha_2 = \dfrac{R_4}{R_3 + R_4}$, $\beta_2 = \left(\dfrac{W}{L}\right)_6 \Big/ \left(\dfrac{W}{L}\right)_5$, taking (9) into (10) can get:

$$V_N = \frac{\left(1 - \sqrt{\beta_2}\right)}{1 - \alpha_2\left(1 + \sqrt{\beta_2}\right)} V_{thn} \tag{11}$$

Also, carrier mobility μ is offset; α_2 and β_2 can be considered to be constants independent of temperature. Because V_{thn} is linear with temperature, so voltage V_N whose value can be adjusted by setting different α_2 and β_2 is a linear function about temperature. It needs to be noted that the impact of body effect on M5 threshold voltage is ignored to simplify the calculation. However, even considering the body effect, it only needs to modify V_{bseff} in (3). V_{thn} remains a linear relationship with temperature although V_{thn} temperature coefficient is changed.

Design of Weighted Summation Circuit

By (8) and (11) can be seen that V_P and V_N are both negative temperature coefficient, so the weighted summation circuit can be achieved by subtractor. As shown in FIG.2, the weighted summation circuit is constituted by R5, R6, R7 and operational amplifier A3. Because A3 works in the deep negative feedback state, so the potential of non-inverting terminal is equal to that of inverting terminal. Apply KCL law to R5 ~ R7 parallel nodes：

$$\frac{V_N - V_P}{R_5} = \frac{V_P}{R_6} + \frac{V_P - V_{REF}}{R_7} \tag{12}$$

Through simplification, the subtractor low frequency transfer function is:

$$V_{REF} = \frac{R_7}{R_5}\left[\left(1 + \frac{R_5}{R_6} + \frac{R_5}{R_7}\right)\cdot V_P - V_N\right] \tag{13}$$

The V_{REF} temperature coefficient is：

$$\frac{\partial V_{REF}}{\partial T} = \frac{R_7}{R_5}\left[\left(1 + \frac{R_5}{R_6} + \frac{R_5}{R_7}\right)\cdot \frac{\partial V_P}{\partial T} - \frac{\partial V_N}{\partial T}\right] \tag{14}$$

It is easy to see if don't consider temperature drift caused by operational amplifier disorder, we can make temperature coefficients of V_P and V_N equal and offset through reasonably setting α_1、α_2、β_1、β_2 and values of R5 ~ R7.Thereby V_{REF} becomes a reference voltage which has theoretical zero temperature coefficient and can be adjusted by selecting R7 and R5 resistance ratio.

Design of Operational Amplifier

In previous discussion, in order to make (6) and (9) correct, operational amplifiers work in the deep negative feedback state. The operational amplifiers require high open-loop gain to ensure that conditions in actual design. At the same time, in order to further improve the accuracy, stability of reference voltage and increase output range as far as possible, operational amplifiers also need high common mode rejection ratio and wide linear range. Therefore, a folded-cascode structure as shown in FIG.3 is selected. Besides amplifier stage, the bias of static current also adopts cascode structure to offset fluctuations of supply voltage V_{analog} and enhance stability; M15 and M16 constitute PMOS differential pair to expand input voltage range; M17, M18 and M21 , M22 provide the bias current to secondary cathode-input amplifier, at the same time, as high- impedance active load, they improve the open-loop gain; Output terminal uses PMOS M27 as a source follower to reduce the output impedance and improve output voltage swing; In order to make operational amplifiers work stably in high gain and wide linear range, C1 is used in this circuit to compensate frequency. Verified by simulation, the open-loop gain reaches 105db, CMRR and PSRR are above 150db, open-loop bandwidth is around 10 kHz, which ensures the accuracy, range and stability of output reference voltage.

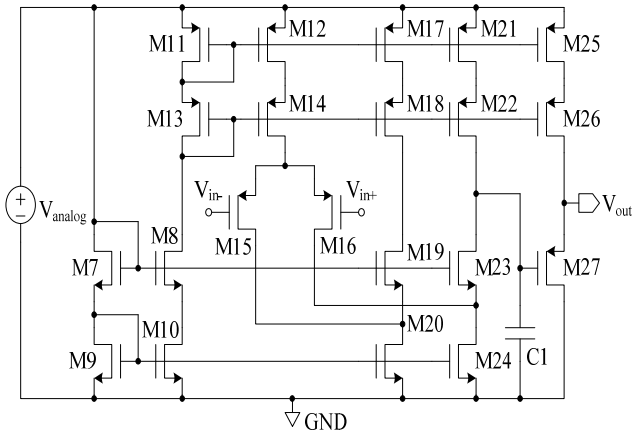

FIG.3 OPERATIONAL AMPLIFIER CIRCUIT

Device Parameters Design

Based on the above analysis, this circuit is designed based on the 0.5μm CMOS process. Because the folded-cascode amplifier in circuit is typical operational amplifier, so only parameters of M1 ~ M6 and R1 ~ R7 are given in TABLE 1. The pairs of M3, M4 and M5, M6 are all designed to have same channel width.

TABLE 1 PART OF THE DEVICE PARAMETERS

Device	Width/ μm	Length/ μm	Device	Resistance /KΩ
M1	1	20	R1	60
M2	1	15	R2	120
M3	2.4	24	R3	120
M4	2.4	3.6	R4	60
M5	6	54.6	R5	50
M6	6	3.6	R6	124.5
			R7	144.275

It is necessary to increase size appropriately and try to place devices in adjacent locations to reduce lithography error and enhance the matching. Channel width to length ratio of M1 and M2 are relatively small, in order to minimize start-up losses.

Simulation Results and Discussion

Simulation Results

The reference voltage source is simulated by Hspice, and the relevant results are shown in FIG. 4 and FIG.5. As can be seen from FIG.4, under the condition of the input voltage is 3.6 V, when environment temperature changes from -50 ° C to +150 ° C, reference voltage V_{REF} only changes from 1.218V to 1.228V. This circuit significantly reduces the error caused by nonlinear of triode V_{BE} in conventional band-gap reference and shows a fairly good temperature characteristics, the temperature coefficient is:

$$TC_F = \frac{\Delta V_{REF}}{\Delta T \cdot V_{REF}} = \frac{1.228 - 1.218}{1.22 \times (150 + 50)} = 40.9 \times 10^{-6}/K \quad (15)$$

From FIG.5, we can see that V_{REF} only changes from 1.221 V to 1.222 V when power supply voltage V_{analog} is from 3 V to 4.2 V. Obviously, the circuit has better power supply rejection characteristic. According to the above parameters, the sensitivity of reference voltage to the power supply voltage fluctuations is given by: $S_{V_{analog}}^{V_{REF}} = \frac{\Delta V_{REF}/V_{REF}}{\Delta V_{analog}/V_{analog}} = \frac{(1.222 - 1.221)/1.22}{(4.2 - 3.0)/3.6} = 0.246\%$ (16)

In addition, the value of the reference voltage source can be adjusted arbitrarily, thus, the flexibility of designing circuit is increased greatly.

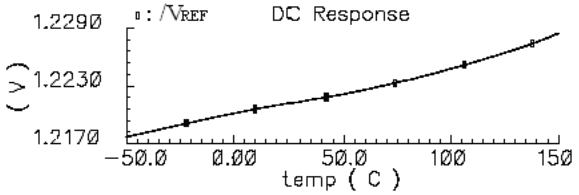

FIG.4 WAVEFORM OF REFERENCE VOLTAGE VARIES WITH TEMPERATURE

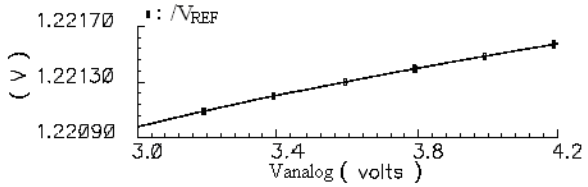

FIG.5 WAVEFORM OF REFERENCE VOLTAGE VARIES WITH SUPPLY VOLTAGE VANALOG

Discussion of Offset Voltage in Operational Amplifier

In order to ensure the correctness of (6) and (9), the input offset voltage of op-amp is not considered in the above analysis. Actually, the input offset voltage has an important influence on the performance of reference voltage source. Especially in CMOS process, the problem of offset voltage is more serious than bipolar process, the analysis is as follows. Firstly, assuming the input offset voltages of A1~A3 are V_{OS1}, V_{OS2} and V_{OS3} respectively, take A1 as an example, Equation (6) becomes:

$$V_{a'} \approx V_a + V_{0S1} = \frac{R_2}{R_1 + R_2} V_P + V_{0S1} = \alpha_1 \left(V_P + \frac{1}{\alpha_1} V_{0S1} \right) \qquad (17)$$

This can be seen as A1 works without offset , the output voltage increases（V_{OS1}/α_1）compared with previous, so：

$$V_P = \frac{1 - \alpha_1 (1 + \beta_1) + (1 - \alpha_1)\sqrt{1 + \beta_1}}{1 - \alpha_1^2 (1 + \beta_1)} V_{thp} + \frac{V_{0S1}}{\alpha_1} \qquad (18)$$

Due to $V_{OS1} \ll V_{thp}$, V_{OS1} has less effect on V_P, we can appropriately increase α_1 to further reduce the effects of V_{OS1}. But at the same time, the linear coefficient of V_{thp} is changing, so the design needs to be balanced. When the ratio of polynomial contains V_{OS1} to polynomial contains V_{thp} is the minimum in possible range, the influence caused by offset voltage is the least. Similarly, for A2 and A3, (11) and (13) respectively become:

$$V_N = \frac{\left(1 - \sqrt{\beta_2}\right)}{1 - \alpha_2 \left(1 + \sqrt{\beta_2}\right)} V_{thn} + \frac{V_{0S2}}{\alpha_2} \qquad (19)$$

$$V_{REF} = \frac{R_7}{R_5} \left[\left(1 + \frac{R_5}{R_6} + \frac{R_5}{R_7} \right) \cdot \left(V_P + V_{0S3} \right) - V_N \right] \qquad (20)$$

The analysis of the influence of V_{OS2} on V_N is identical with that of V_{OS1} on V_P. As can be seen from (20),by using a weighted subtraction to V_P and V_N , and selecting appropriate value of R5 ~ R7 and α_1、α_2 , circuit can partially or even largely counteract the influence caused by offset voltage. Therefore, trimming can be increased to adjust them in layout design.

Conclusions

The reference voltage source based on the standard CMOS process is described in this paper. According to the linear relationship between temperature and the threshold voltages of NMOS and PMOS, V_P and V_N are obtained, which are not only independent of the power supply and mobility, but also change linearly with the threshold voltages of PMOS and NMOS. Then an adjustable reference voltage can be obtained by subtracting two voltages to offset the temperature coefficient. The designed circuit makes static power consumption and layout area reduced and fundamentally overcomes the problem that the temperature coefficient of base-emitter junction voltage V_{BE} is nonlinear in conventional band-gap reference. Its performance has been verified reaching the design goal by Hspice simulation. This circuit is successfully applied to a Buck converter, the measured results are in accordance with theory, which proves the scheme is correct and feasible.

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